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1. Single-Photon Source Integration to Silicon Photonics for Scalable Quantum Processing

Date Posted	22 Dec 2025	
Home University	Nanyang Technological University	
Partner University	Sungkyunkwan University	
Supervisors	**Home**	**Partner**
Name	Chae Sanghoon	Hyeon Suk Shin
School	School of Electrical and Electronic Engineering	Department of Energy & Department of Chemistry, SKKU
Email	sanghoon.chae@ntu.edu.sg	shin0902@skku.edu
Website	https://sites.google.com/view/sanghoonchae/home	https://www.ibs.re.kr/2dqh/
Project Description (200-300 words)	Deterministic single-photon sources are essential for photonic quantum technologies, including quantum computing, secure communications, and quantum sensing. Silicon photonics offers a scalable and CMOS-compatible platform for large-scale quantum photonic integration, yet the on-chip realization of high-quality single-photon emitters remains a critical challenge. This project focuses on the integration of van der Waals (vdW) quantum emitters, particularly defect-based single-photon sources in hexagonal boron nitride (hBN), into silicon and silicon nitride photonic circuits. hBN hosts optically stable quantum emitters that operate at room temperature and can be deterministically positioned, making it an attractive platform for scalable quantum photonics. The project will explore hybrid integration approaches, including vdW material transfer, nanophotonic cavity coupling, and waveguide-embedded architectures, to enhance emission efficiency and on-chip photon collection. Comprehensive optical characterization will be performed using photon correlation measurements, lifetime analysis, and on-chip interference experiments to evaluate single-photon purity, brightness, and coherence. By combining vdW quantum materials with mature silicon photonics, this research aims to establish a practical pathway toward scalable, integrated quantum photonic processors based on deterministic single-photon sources.	
Program/Center Website(s)	Centre for Micro- & Nano-Electronics (CMNE) https://www.ntu.edu.sg/cmne	

Additional Information (e.g., files with project details)	N.A

2. Ferroelectric-integrated silicon photonics for non-volatile reconfigurable optical computing

Date Posted	3 Nov 2025	
Home University	Nanyang Technological University	
Partner University	Sungkyunkwan University	
Supervisors	**Home**	**Partner**
Name	Chae Sanghoon	Kim Yunseok
School	School of Electrical and Electronic Engineering	School of Advanced Materials Science and Engineering
Email	sanghoon.chae@ntu.edu.sg	yunseokkim@skku.edu
Website	https://sites.google.com/view/sanghoonchae/home	https://sites.google.com/view/yunseokkim
Project Description (200-300 words)	The rapid growth of artificial intelligence and data-intensive computing has driven the need for energy-efficient hardware capable of performing computation and memory functions directly in the optical domain. Conventional silicon photonic circuits, while mature and CMOS-compatible, lack intrinsic non-volatility and reconfigurability, limiting their potential for in-memory and adaptive optical computing. This PhD project aims to develop a new class of non-volatile, reconfigurable photonic platforms by integrating ferroelectric materials with silicon photonics. The research will focus on incorporating ferroelectric materials into silicon nitride and silicon photonic devices. Leveraging their spontaneous polarization and electric-field tunability, these materials will enable persistent refractive index modulation without static power consumption. The project will investigate the underlying ferroelectric switching mechanisms, interface engineering for low-loss optical coupling, and scalable fabrication processes compatible with wafer-scale integration. Through this program, the candidate will implement dynamically reconfigurable optical neural networks and logic circuits by designing and demonstrating ferroelectric-based phase modulators, modulators, and photonic memory devices. This research combines NTU's cutting-edge photonic device technology with SKKU's ferroelectric materials and measurement techniques. By merging materials science, nanofabrication, and integrated optics to establish ferroelectric-integrated silicon photonics as a key component of next-generation energy-efficient optical computing systems, this research will advance the state-of-the-art in photonic in-memory computing.	

Program/Center Website(s)	Centre for OptoElectronics and Biophotonics (COEB): https://www.ntu.edu.sg/coeb
Additional Information (e.g., files with project details)	N.A

3. Integrating Micro-LEDs into Si Photonics for Frontier Optical Interconnect Networks

Date Posted	16 Sep 2025	
Home University	Nanyang Technological University	
Partner University	Sungkyunkwan University	
Supervisors	**Home**	**Partner**
Name	Chae Sanghoon	Young Joon Hong
School	School of Electrical and Electronic Engineering	SAINT (SKKU Advanced Institute of Nano Technology)
Email	sanghoon.chae@ntu.edu.sg	yjhong78@skku.edu
Website	https://sites.google.com/view/sanghoonchae/home	https://sites.google.com/view/snadatsejong
Project Description (200-300 words)	The growth of artificial intelligence (AI) and data-intensive computing industries has pushed electronic interconnects to their limits related to bandwidth, energy efficiency, and latency. For sustainable high-performance computing, new optical interconnect solutions are needed. This project presents an innovative approach to build cutting-edge optical interconnect networks by integrating micro-LEDs into silicon photonic platforms. Unlike conventional laser-based systems, micro-LEDs have exceptional advantages including miniaturization, wavelength diversity, active electrical control, and seamless CMOS compatibility. This integration enables massive parallel processing through simultaneous multi-wavelength operation. It also provides cost-efficient scalability via wafer-level manufacturing processes. Our research aims to systematically address key technical challenges. First, we implement optimized optical pathways through advanced on-chip silicon photonic waveguide design based on simulation. Additionally, we develop active modulation systems with enhanced bandwidth by utilizing external electro-optic control. Furthermore, we strategically utilize photonic cavities such as microring resonators and photonic crystal structures to dramatically enhance signal strength through Purcell effect and resonance. Consequently, this technology will facilitate a paradigm shift toward photonic-electronic co-design architectures and establish new industry standards. This breakthrough technology will fundamentally transform how future systems communicate information and enable next-generation computing platforms spanning autonomous systems, edge computing, and quantum interconnects.	

Program/Center Website(s)	Centre for Micro- & Nano-Electronics (CMNE) https://www.ntu.edu.sg/cmne
Additional Information (e.g., files with project details)	N.A

4. Nonvolatile Integrated Photonics for Edge Neuromorphic Computing

Date Posted	04 Aug 2025	
Home University	Nanyang Technological University	
Partner University	Sungkyunkwan University	
Supervisors	**Home**	**Partner**
Name	Chae Sanghoon	Lee Sungjoo
School	School of Electrical and Electronic Engineering	SAINT (SKKU Advanced Institute of Nano Technology)
Email	sanghoon.chae@ntu.edu.sg	leesj@skku.edu
Website	https://sites.google.com/view/sanghoonchae/home	https://sites.google.com/view/skku-ndtl/home
Project Description (200-300 words)	Advancements in nonvolatile photonic memory are critical for next-generation edge AI and neuromorphic computing, enabling real-time inference in applications such as IoT, biosignal decoding, and time-series forecasting. This project explores the integration of ferroelectric materials into photonic neuromorphic architectures to develop ultra-fast, energy-efficient, light-based neural networks. By leveraging analog in-memory photonic computing, our approach overcomes the limitations of electronic AI accelerators, offering unmatched scalability, low latency, and power efficiency for intelligent edge devices in robotics, autonomous systems, and distributed sensing. A key innovation of this work is the fusion of emerging materials science with applied neuromorphic photonics. We propose integrating ferroelectric materials and tunable 2D nonlinear optics into silicon photonic platforms, creating a reconfigurable framework for high-speed, parallel, and adaptive processing. This hybrid architecture addresses critical challenges in edge AI, such as dynamic learning, energy constraints, and real-time adaptability, paving the way for deployable photonic neuromorphic systems.	
Program/Center Website(s)	Centre for OptoElectronics and Biophotonics (COEB): https://www.ntu.edu.sg/coeb	
Additional Information (e.g., files with project details)	N.A	

5. Development of 2D/3D heterointerface on nanostructured Si to exceed quantum efficiency beyond limits

Date Posted	1 July 2024	
Home University	Nanyang Technological University	
Partner University	Sungkyunkwan University	
Supervisors	**Home**	**Partner**
Name	Kim Munho	Kang Joohoon
School	School of Electrical and Electronic Engineering	Department of Advanced Materials Science & Engineering
Email	munho.kim@ntu.edu.sg	joohoon@skku.edu
Website	https://ntunedl.weebly.com/	https://sites.google.com/view/mfmp/home
Project Description (200-300 words)	Our project represents a pioneering study on completely new hybrid-type optoelectronic devices that combine two different materials: two-dimensional (2D) thin films coated on three-dimensional (3D) nanostructured black silicon (b-Si). Further advancement in the device performance will be achieved through the investigations on the conformal coating of 2D materials onto 3D nanostructures, 2D/b-Si heterointerface, and interface passivation via plasma treatment. Unlike traditional 3D devices, the combination of 2D and 3D materials creates a unique junction with exceptional thermal and electrical conductivity and remarkable responsivity. However, 2D/3D heterostructures face challenges such as limited light absorption and high interface defect density, which affect device performance. Our project aims to overcome these hurdles by combining 2D/3D heterojunction technology, nanostructured b-Si, and novel plasma-based interface passivation into a single device. Our approach involves conformally coating a 2D monolayer onto nanostructured b-Si via direct growth method, creating nanotextured b-Si, and passivating the surface using plasma treatment. The success of our project will lay the foundation for future technologies, including biosensors and optical communication systems. Importantly, our device is compatible with current complementary metal-oxide-semiconductor (CMOS) technology, enabling integration with advanced CMOS devices and circuits like CMOS image sensors. This extends the impact of our innovation beyond Singapore to the global stage. Additionally, our research has the potential to generate new knowledge on carrier transport mechanisms, heterointerface, and photomultiplication across 2D/3D interfaces, contributing to a deeper understanding of these phenomena.	
Program/Center Website(s)	https://www.ntu.edu.sg/coeb	

Additional Information (e.g., files with project details)	The project can be summarized into four self-contained yet interconnected work packages (WPs). WP1 is the fundamental study of the coating process for large size defect-less graphene (Gr) and hexagonal boron nitride (hBN), and the nanotexturing process of b-Si, involving plasma treatment passivation. WP2 will focus on the formation of passivated 2D/3D heterointerface on a nanostructured b-Si. This will be achieved through two key methodologies: the direct growth of 2D layers and Cl-based plasma passivation. Based on the successful implementation of WP1 and WP2, WP3 will perform theoretical and experimental study of the heterointerface. Particular attention will be paid to understanding carrier recombination dynamics within our 2D/3D heterojunction nanostructures. Building on the theoretical and practical insights gained in the preceding WPs, WP4 focuses on the development of high-performance self-powered devices with superior quantum efficiency. The aim is to implement the knowledge to further enhance device performance through refinement and innovative strategies. Following figure provides a visual representation of the implementation plan across the four WPs.