Time-predictable hardware platforms

Due to increasing complexity and the need to consolidate functionality onto fewer hardware, the computational demand of cyber-physical real-time systems is steadily rising. Commercial-Off-The-Shelf (COTS) multi-core processors are a natural choice to meet this demand due to their superior Size, Weight & Power (SWaP) characteristics. But they are unsuitable for use in real-time systems, because executions on these platforms are not worst-case predictable. The main reason for this unpredictability is the various hardware shared between cores such as caches, on-chip interconnect, and memory controllers.

To use a hardware in real-time systems, the Worst-Case Execution Time (WCET) of applications executing on the hardware should be computable. We are developing a System-on-Chip architecture based on Commercial-Off-The-Shelf multicores, focusing on the design of a time-predictable memory hierarchy. Xilinx Zynq 706 platform is used to demonstrate the feasibility of the architecture.

The main activities of the project can be summarized as follows:

- Experimental evaluation of existing COTS multi-cores to show that worst-case predictability is infeasible.
- Design and analysis of predictable shared caches, including replacement and coherency policies.
- Design and analysis of predictable memory controller, including arbitration policy.
- Design and analysis of predictable inter-core interconnect, including arbitration policy.
- Validation of the proposed hardware architecture in terms of predictability and SWaP characteristics using safety-critical applications.

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