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Technology Offer

Dual-path Sub-Sampling PLL with Feedback Phase Noise Cancellation Technique

Technology Overview

Ring voltage-controlled oscillator (VCO) based PLLs have several advantages over LC-VCO based PLLs, like smaller chip area, wider frequency tuning range and multi-phase output signals. However, the inferior jitter/phase noise of ring VCOs has always been the bottleneck of the overall PLL jitter/phase noise performance. To suppress ring VCO's phase noise, feedforward phase noise cancellation (FFPNC) techniques and feedback phase noise cancellation (FBPNC) technique are widely researched. Most FFPNC and FBPNC based structures require numerous additional blocks, which consumes significant extra area and power. In order to suppress phase noise of the ring VCO with minimal area and power consumption, this technology offers a dual-path ring VCO based sub-sampling PLL (SSPLL) with a FBPNC technique.

Technology Features / Specifications

The main structure of this design is based on the conventional SSPLL, which intrinsically eliminates divider noise and reduces the phase detector (PD)/charge pump (CP) noise by the multiplication of N^2. Therefore, the PLL phase noise is mainly decided by the reference and ring VCO. The architecture of the proposed dual-path SSPLL is shown in Figure 1, which includes a sub-sampling loop and a frequency-locked loop. Compared to the conventional SSPLL, the main difference is the dual-path structure from the output of the SSPD to the low-pass filter (LPF). One path from the SSPD to the LPF is through sub-sampling charge pump 1 (SSCP1), the other path is composed of the high-pass filter (HPF) and SSCP2. The SSPD samples the ring VCO's output and then hen the sampled output voltage is converted to an output current by the SSCP1 in path I. In path II, the sampled output is firstly high-pass filtered. Next, the filtered signal is also converted to a current signal and flows into the LPF. These two paths are operating simultaneously to control the LPF. Through properly setting the HPF's high-pass frequency corner and SSCPs' transconductances, a new in-band zero and pole are generated to enlarge the PLL bandwidth. Moreover, since the frequency of the introduced zero is smaller than the pole, the phase margin (PM) of the PLL is compensated. Consequently, the phase noise of the ring VCO contributed to the PLL is suppressed while the loop stability is still ensured.

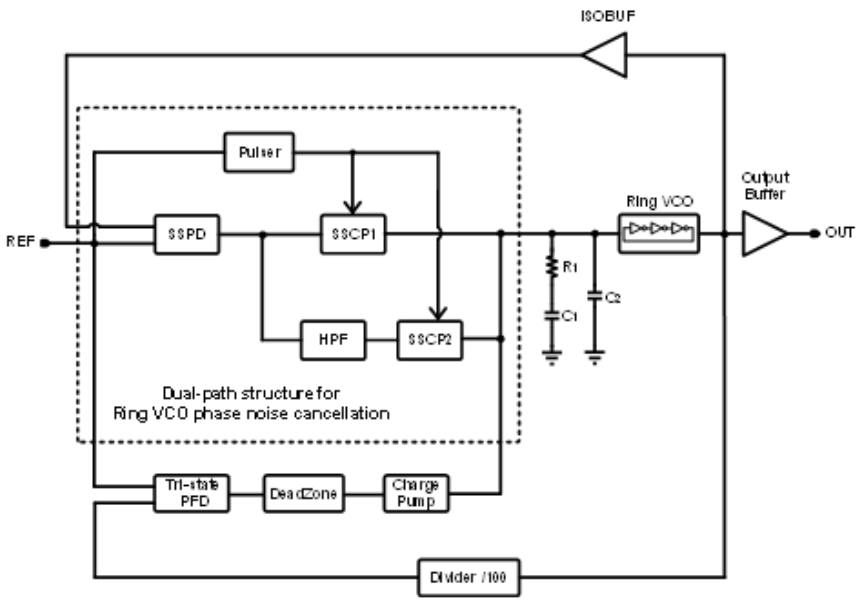

Figure 1. Architectures of the proposed dual-path sub-sampling PLL

The prototype chip with the proposed technology is fabricated in a standard 28nm CMOS technology. The left part of Figure 2 shows the measured phase noise of the proposed SSPLL when $g_{m,SSCP2} = 1.2g_{m,SSCP1}$. Compared to the conventional SSPLL, the phase noise is suppressed from 300kHz to 3.7MHz. The maximum phase noise suppression is 6.5dB@1.1MHz and the jitter integrated from 1kHz to 100MHz is improved from 3.52ps to 2.63ps. The closed-loop bandwidth is enlarged to around 6MHz. The right part of Figure 2 shows the measured results when $g_{m,SSCP2}$ is set as $1.5g_{m,SSCP1}$ by changing the current mirror ratio (the simulated PM is degraded from 60° to 57°). The phase noise is suppressed from 200kHz to 4.1MHz compared to the conventional SSPLL. The maximum phase noise reduction is 7.3dB@1.13MHz and the integrated jitter is improved from 3.52ps to 2.66ps. The closed-loop bandwidth is enlarged to around 7.2MHz.

This technology does not require any additional delay line, clock generation or calibration circuits for the phase noise cancellation path. Furthermore, the cancellation path effectively improves the phase noise performance of the PLL and only consumes 160µW power.

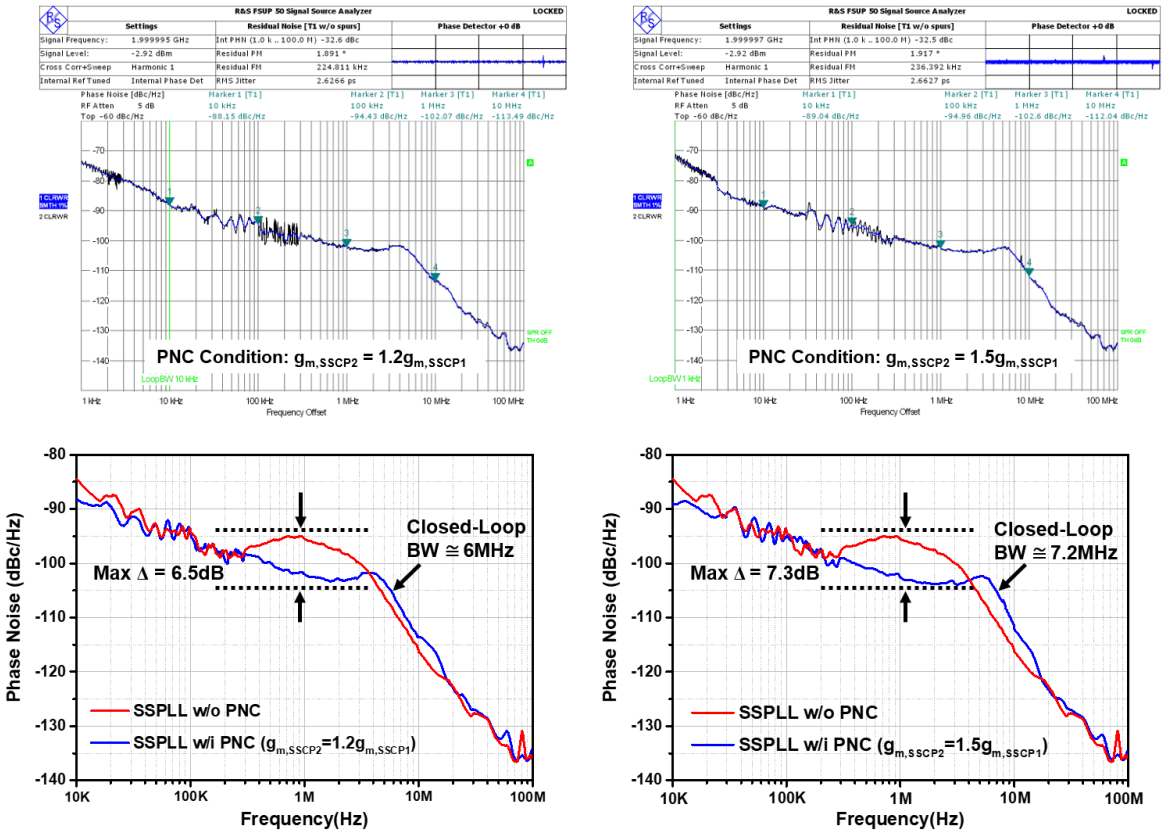

Figure 2. Measure phase noise of the proposed SSPLL compared to the conventional

Potential Applications

Firstly, this technology is suitable to provide local oscillator signals for low-power and small-area sub-6 GHz wireless transceivers.
Secondly, this technology is suitable to provide clock signals for low-power system-on-chips (SoCs) applications.
Thirdly, this technology is also suitable for low-power wireline communication systems.

Benefits

1) The existing PNC techniques always require additional voltage-controlled delay line, clock generation or calibration circuits. For the invented FBPNC technique, the implementation is much simpler, which only requires an additional HPF and SSCP. As a result, it largely simplifies the design process and scales down the die area.
2) Compared to several mW power consumption for the existing FBPNC techniques (e.g. 4mW for the FBPNC technique in [1]), the power consumption for the invented FBPNC technique only comes from the SSCP2, which is 160 µW. The power consumption can be drastically reduced to 4% of the existing FBPNC.
3) The VCO phase noise is effectively suppressed by the invented FBPNC technique while the loop stability is also ensured due to the phase margin compensation effect. For example, in the proposed SSPLL design, the phase noise could be improved by 6.5dB@1.1MHz while the phase margin is not decreased and kept at 60°.

Reference: [1] H. Ting et al., "A 5.25GHz Subsampling PLL with a VCO-Phase-Noise Suppression Technique," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 390-392.

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