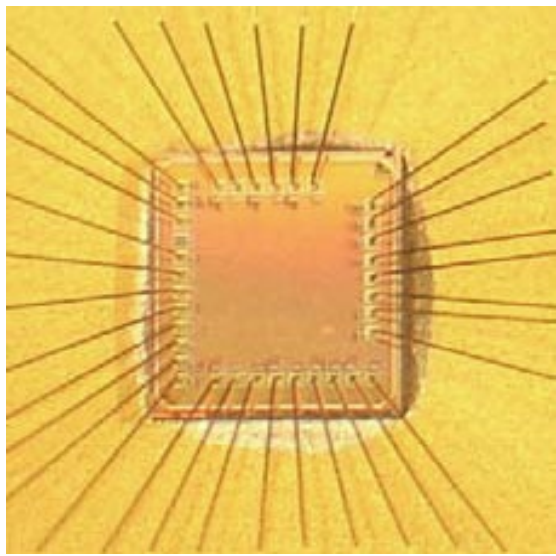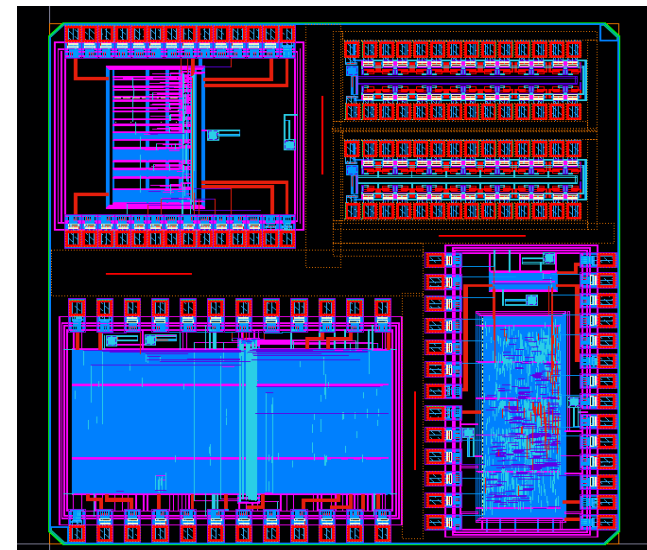# Rad-Hard By Design and Radiation Testing for ICs and SoCs

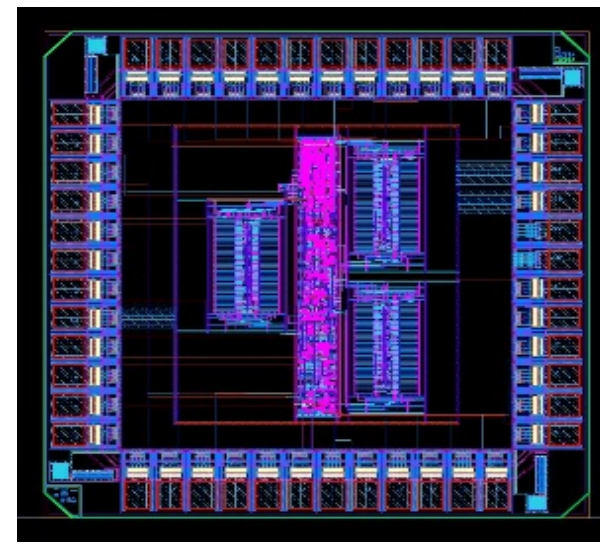## Products and Services

Latchup Protection

Cell Test Structures

TMR Memory
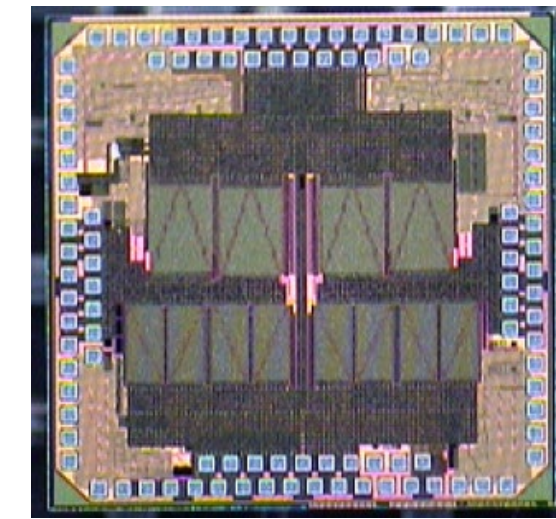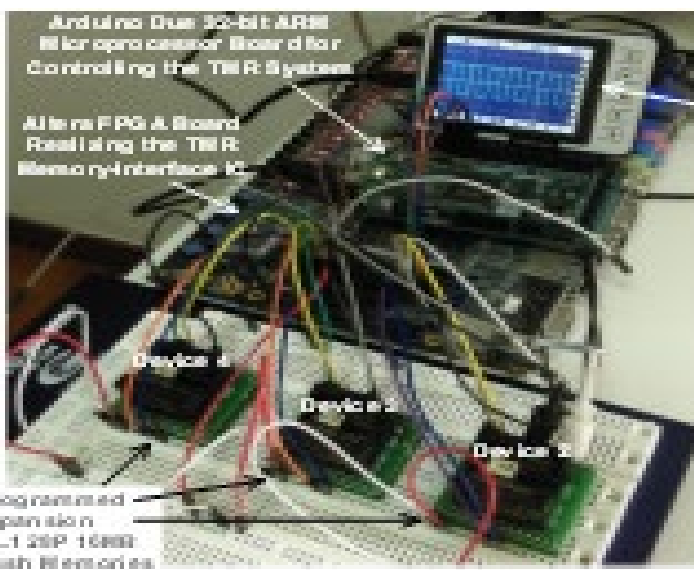

Point-of-Load
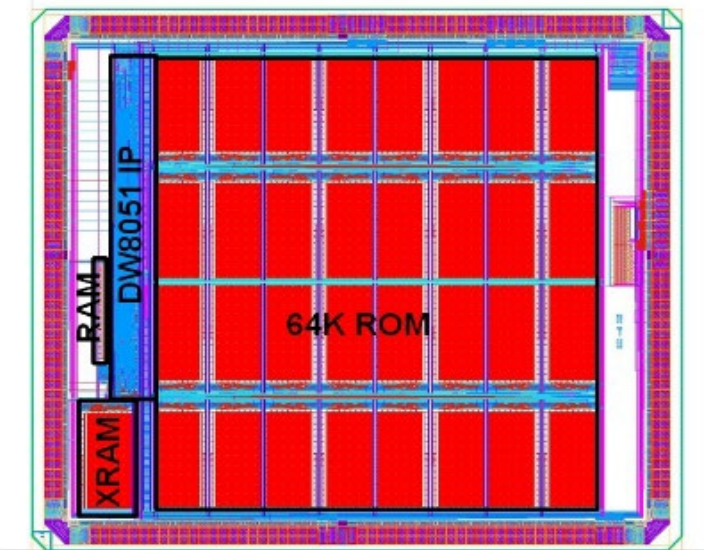
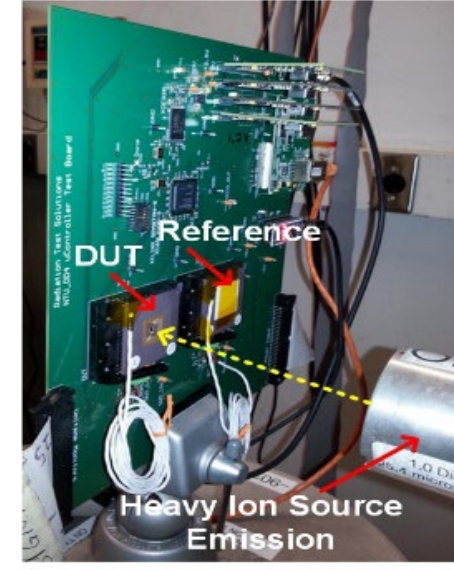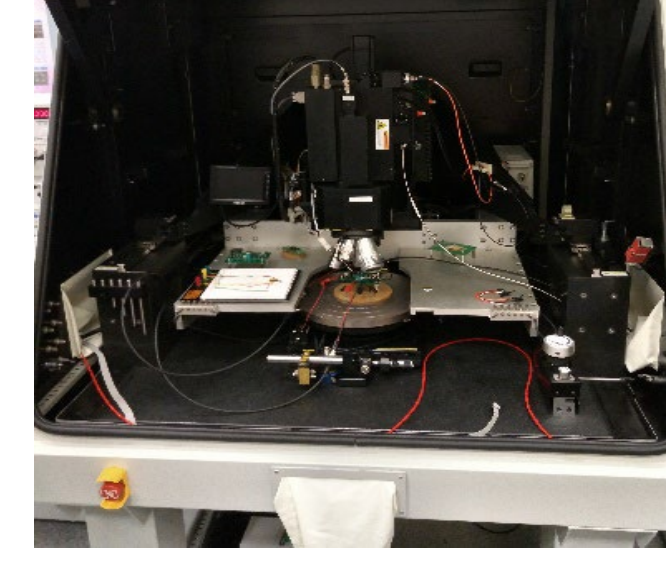
µController

TMR Testing

TID Testing

SEU/SET Testing

Laser Testing

SEL Testing

Product #1
Latchup Detection & Protection

- ❑ Two patents awarded
- ❑ **$10^2 – 10^6$ higher protection over present practice**
- ❑ Detection of the Single-Event-Latchup occurrence in the early stage
- ❑ Detection of micro-Single-Event-Latchup (calibration is required)
- ❑ Protection of COTS ICs from destructive damage by power cycling

- ❑ Total-Ionizing-Dose-free up to 500 Krad(Si)
- ❑ Immune from current drift due to aging and Total-Ionizing-Dose
- ❑ Single-Event-Latchup-free up to LET = 72 MeV·cm²/mg

Product #2
Point of Load (PoL)

- ❑ One pending patent
- ❑ **Maximum power efficiency over all loading conditions**
- ❑ Ultra-fast transient response
- ❑ High step-down ratio >20:1
- ❑ Independent parallelism with redundancy
- ❑ Zero Voltage Switching and Zero Current Switching
- ❑ Minimized passive components

- ❑ Total-Ionizing-Dose-free up to 100 Krad(Si)
- ❑ Latchup-free up to LET = 72 MeV·cm²/mg
- ❑ Single-Event-Transient-free up to LET = 50 MeV·cm²/mg (<100mV)

Product #3
Radiation-Hardened Library Cell

- ❑ Four pending patents
- ❑ **3.5x better power-delay-area product than the state-of-the-art**
- ❑ 47 Rad-Hard combinational cells @ 65nm CMOS
- ❑ 11 Rad-Hard sequential cells @ 65nm CMOS

- ❑ Total-Ionizing-Dose-free up to 100 Krad(Si)
- ❑ Single-Event-Transient-free up to LET = 10 MeV·cm²/mg
- ❑ Standalone flip-flop with SEU error rate @ GEO <4.6x10⁻¹⁰ error/bit/day
- ❑ Redundancy flip-flop with SEU error rate @ GEO <1.0x10⁻¹³ error/bit/day
- ❑ Latchup-free up to LET = 50 MeV·cm²/mg

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